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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,890	05/12/2005	Francesco Alex Maone	CH02 0035 US	3568

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EXAMINER	
MA, CALVIN	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,890	MAONE ET AL.	
	Examiner	Art Unit	
	CALVIN C. MA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arnaud (USP. 4989242) in view of MacNally (USP. 6,516,185).

As to claim 1, Arnaud teaches an apparatus for processing a differential input signal (i.e. differential voltage v1 which is based on audio information) (see Col. 6, Lines 1-15), the apparatus comprising a peak detector with a differential input (i.e. the circuitry detect sounds function to detect peak in signals with a wide range of values that is differential in nature), the peak detector configured to provide a first voltage being proportional to an average voltage peak at the peak detector's differential input (i.e. the first voltage is the voltage signal before attenuation and voltage gain via the amplifier), a compressor processing (GE) the first voltage in order to provide a second voltage (voltage outputted form G1), a voltage controllable current source configured to provide a trim current being adjustable by the second voltage (i.e. voltage current converter 31), a hysteresis equipped circuit, wherein the peak detector is operationally coupled to the compressor and the compressor is operationally coupled to the voltage controllable

current source (i.e. the hysteresis HYST1 depends upon the gain variation dG1 which is affected by the current source changes where the compressor GE is ultimately influential to the downstream components requiring the adaptive hysteresis which is provided for at the active emission or reception input of amplifier A3) (see Fig. 2,4, Col. 6, Line 1-Col.7, Line 27).

However, Arnaud does not explicitly teach the hysteresis circuit having hysteresis characteristics, the hysteresis equipped circuit configured to adjust the hysteresis circuit responsive to the trim current (Arnaud does teach that the hysteresis circuit being applied in the drawing of figure 4 where the hysteresis circuit is used to help the comparator to make the correct detect to prevent chopping of speech signals). MacNally teaches the hysteresis circuit having hysteresis characteristics, the hysteresis equipped circuit configured to adjust the hysteresis circuit responsive to the trim current (i.e. as seen in figure 3 of MacNally the counter/hysteresis unit 352 evaluates the changes of the signal that move within a range for example 0.15 to 1.6 Vp-p, this means a current signal which is the flow of electron based on the voltage differential exists and is detect, therefore the counter hysteresis circuit is responsive to the trim current that is detected) (see MacNally Fig. 3, Col. 6, Lines 20-50).

Therefore it would have been obvious for one of ordinay skill in the art at the time the invention was made to have used the counter/hysteresis circuit of MacNally in the overall system of Arnaud in order to allow Arnaud's correction design to function in a digital signal correct system to extend it field of application of communication system in general.

As to claim 2, Arnaud teach the apparatus of claim 1, wherein the peak detector comprises an integrator (IE) (i.e. in figure 1 Arnaud clear shows that the peak detector contains integrator, even though this is cited as prior art it still demonstrate that peak detector can have an integrator) (see Fig. 1).

As to claim 3, Arnaud teaches the apparatus of claim 1, wherein the peak detector operates on the envelop of a differential input signal being applied to the differential input (i.e. the peak detection capability of the hysteresis based circuit works by being applied to the differential AC voltage signal which creates an envelop) (see Fig. 2) (Col. 4, Lines 15-40).

As to claim 4, Arnaud teaches the apparatus of claim 1, wherein the peak detector is designed to constantly follow the average voltage peak at the peak detector's differential input (i.e. the noise compensation design of the circuit means that the peak detector follow the average peak and compensate for the shift in noise signals) (See Col. 8, Lines 30-60).

As to claim 5, Arnaud teaches the apparatus of claim 1, providing a hysteresis characteristics depending on the average voltage peak at the peak detector's differential input (i.e. since the circuits functions as a multiplier substractor controlling the noise level, the hysteresis characteristic are adjust based on the levels of the differential signal where the high noise is controlled accordingly) (see Fig. 5, Col. 8, Lines 30-55).

As to claim 6, Arnaud teaches the apparatus of claim 1, wherein the peak detector comprises a differential input transistor pair (T1, T2) at its differential input (i.e. the pair of PNP transistor T1 and T2) (see Fig. 5, Col. 7, Lines 45-50).

As to claim 7, Arnaud teaches the apparatus of claim 6, wherein the load conditions of the differential input transistor pair (T1 T2) changes when the average voltage peak changes (i.e. the differential input transistor pair is connected to two other transistor T3 and T4 which changes when the voltage peak changes affecting the load of T1 and T2) (see Fig. 5, Col. 7, Lines 43-67).

As to claim 8, Arnaud teaches the apparatus of claim 1, wherein the hysteresis characteristics are adjusted by shifting trip-levels of the hysteresis equipped circuit to lower levels if the differential input signal is a low level signal and to higher levels if the differential input signal is a high level signal (i.e. since the circuits functions as a multiplier substractor controlling the noise level, the hysteresis characteristic are adjust based on the levels of the differential signal where the high noise is controlled accordingly) (see Fig. 5, Col. 8, Lines 30-55).

As to claim 9, Arnaud teaches the apparatus of claim 1, wherein a differential clock signal is used as the differential input signal to perform a sensing phase and an appropriate adjustment of the hysteresis characteristics (i.e. in the reception mode the hysteresis circuit is changed to adapt to new conditions (see Col. 7, Lines 30-61).

As to claim 10, Arnaud teaches the apparatus of claim 1, wherein the compressor applies a function when processing the first voltage (42) in order to provide

the second voltage (i.e. the function of compressor is to maintain predetermined peak value) (see Fig. 2, Col. 3, Lines 60-67).

3. Claims11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arnaud in view MacNally as applied to claims 1-10 and further in view of Chow (USP 6836149).

As to claim 11, claim 11 is analyzed to differ from claim 1 only in that it adds the limitation of control circuitry for a display system comprising an array of interfaces. Arnaud does not teach control circuitry for a display system comprising an array of interfaces. Chow teaches control circuitry for a display system comprising an array of interfaces (i.e. the interface for RSDS, LVDS, MINILVDS, and BLVDS) (see Fig. 1, Col. 2, Lines 52-67).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to have adapted the hysteresis based error signal reduction circuitry of Arnaud and the hysteresis system for digital communication system of MacNally into the various video interface adapting format of Chow, since it is well know in the art that electronic transmission of signal has similar noise characteristic over common medium such as wires by which both audio and video information pass through.

As to claim 12, Arnaud, MacNally and Chow teaches the control circuitry of claim 11, wherein a signal is provided by the at least one interface (62.1) to other interfaces of

the array of interfaces in order to allow the hysteresis characteristics of the other interfaces to be adjusted, too (i.e. since Chow's system adapt for a variety of different interface and implement the change on the fly with software based system, it would be able to take advantage of the hysteresis based compensation system for the multiple interfaces) (see Chow Fig. 1, Col. 3, Lines 4-57).

As to claim 13, Chow teaches the control circuitry of claim 11, wherein the interfaces of the array of interfaces serve as differential RSDS interfaces (see Chow, Col. 3, Line 40).

As to claim 14, Chow teaches the control circuitry of claim 11, wherein the interfaces of the array of interfaces serve as low EMI/low power interfaces between timing controllers and digital-to-analog latches employed for driving analog signals onto column electrodes of a display panel of the display system (i.e. the BLVDS being a point to point configure creates low EMI/low power interface on to the column electrode of the display) (see Fig. 2, Col. 3, Line 57-Col. 4, Line 15).

As to claim 15, Chow teaches the control circuitry of claim 11 further comprising a transmitting circuit for transmitting video data to the array of interfaces (i.e. the circuitry design can be extended to future high speed video system) (see Fig. 8, Col. 8, Lines 15-19).

As to claim 16, Chow teaches the control circuitry of claim 15, wherein the array of interfaces converts the video data into analog signals for driving onto column

electrodes of a display panel of the display system (i.e. the LCD monitor has column driver that is connected to the display interfaces) (see Fig. 1).

As to claim 17, Chow teaches the control circuitry of claim 14, wherein any kind of reduced swing signaling can be used to transmit the video data to the array of interfaces (i.e. RSDS, LVDS, BLVDS are all different swing signaling) (see Fig. 1, Col. 2, Lines 53-67).

Response to Arguments

4. Applicant's arguments with respect to claims1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN C. MA whose telephone number is (571)270-1713. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Quan-Zhen Wang can be reached on 571-272-3114. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
October 4, 2010

/Quan-Zhen Wang/
Supervisory Patent Examiner, Art Unit 2629